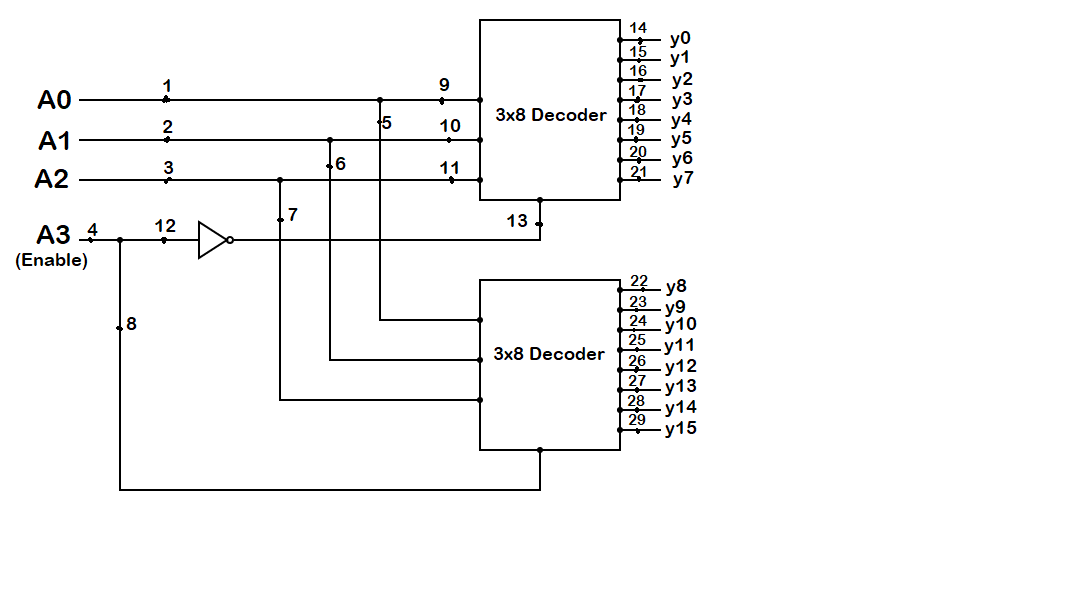
While doing the project we find the following test cases:

As we have to check the Stuck at 1 fault in 4x16 decoder, the circuit diagram is as follows:

As you can see in the figure, we have total 29 possible cases where stuck at 1 fault can be assumed. So, below are the test sets for which output mismatches with the expected output, for corresponding fault positions:

|  |  |
| --- | --- |
| FAULT POSITION | TEST SETS(A3A2A1A0) |
| 1 | 0000 ,0010,0100,0110,1000,1010,1100,1110 |
| 2 | 0000,0001,0100,0101,1000,1001,1100,1101 |
| 3 | 0000,0001,0010,0011,1000,1001,1010,1011 |
| 4 | 0000,0001,0010,0011,0100,0101,0110,0111 |
| 5 | 1000,1010,1100,1110 |
| 6 | 1000,1001,1100,1101 |
| 7 | 1000,1001,1010,1011 |
| 8 | 0000,0001,0010,0011,0100,0101,0110,0111 |
| 9 | 0000 ,0010,0100,0110 |
| 10 | 0000,0001,0100,0101 |
| 11 | 0000,0001,0010,0011 |
| 12 | 0000,0001,0010,0011,0100,0101,0110,0111 |
| 13 | 1000,1001,1010,1011,1100,1101,1110,1111 |
| 14 | 0001,0010,0011,0100,0101,0110,0111, 1000,1001,1010,1011,1100,1101,1110,1111 |
| 15 | 0000,0010,0011,0100,0101,0110,0111, 1000,1001,1010,1011,1100,1101,1110,1111 |
| 16 | 0000,0001,0011,0100,0101,0110,0111, 1000,1001,1010,1011,1100,1101,1110,1111 |
| 17 | 0000,0001,0010,0100,0101,0110,0111, 1000,1001,1010,1011,1100,1101,1110,1111 |
| 18 | 0000,0001,0010,0011,0101,0110,0111, 1000,1001,1010,1011,1100,1101,1110,1111 |
| 19 | 0000,0001,0010,0011,0100,0110,0111, 1000,1001,1010,1011,1100,1101,1110,1111 |
| 20 | 0000,0001,0010,0011,0100,0101,0111, 1000,1001,1010,1011,1100,1101,1110,1111 |
| 21 | 0000,0001,0010,0011,0100,0101,0110, 1000,1001,1010,1011,1100,1101,1110,1111 |
| 22 | 0000,0001,0010,0011,0100,0101,0110,0111, 1001,1010,1011,1100,1101,1110,1111 |
| 23 | 0000,0001,0010,0011,0100,0101,0110,0111, 1000,1010,1011,1100,1101,1110,1111 |
| 24 | 0000,0001,0010,0011,0100,0101,0110,0111, 1000,1001,1011,1100,1101,1110,1111 |
| 25 | 0000,0001,0010,0011,0100,0101,0110,0111, 1000,1001,1010,1100,1101,1110,1111 |
| 26 | 0000,0001,0010,0011,0100,0101,0110,0111, 1000,1001,1010,1011,1101,1110,1111 |
| 27 | 0000,0001,0010,0011,0100,0101,0110,0111, 1000,1001,1010,1011,1100,1110,1111 |
| 28 | 0000,0001,0010,0011,0100,0101,0110,0111, 1000,1001,1010,1011,1100,1101,1111 |
| 29 | 0000,0001,0010,0011,0100,0101,0110,0111, 1000,1001,1010,1011,1100,1101,1110 |

1. Test set for position 4,8 and 12 are same. So, among these 3 positions, two of the positions can be eliminated by applying law of fault equivalence.
2. Test sets for positions 22-29 contain the test sets for position 4 as its subset. So, applying law of fault dominance we can consider the test sets for position 4 as the test sets for these (22-29) positions.
3. Similarly, the test sets for position 14-21 contains the test sets for position 13. So, applying law of fault dominance we can consider the test sets for position 13 as the test sets for these (14-21) positions.
4. Using law of dominance:

Comparing test sets of position 1 and 5, position 5 will dominate.

Comparing test sets of position 2 and 6, position 6 will dominate.

Comparing test sets of position 3 and 7, position 7 will dominate.

Comparing test sets of position 1 and 9, position 9 will dominate.

Comparing test sets of position 2 and 10, position 10 will dominate.

Comparing test sets of position 3 and 11, position 11 will dominate.

1. Repeatedly applying law of dominance, we get the reduced test set as:

{0000,0011,0101,0110,1000,1011,1101,1110}.